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10/804,624	03/19/2004	Don Douglas Josephson	200312720-1	7849

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EXAMINER	
PATEL, DHARTI HARIDAS	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 11/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/804,624	JOSEPHSON ET AL.	
	Examiner	Art Unit	
	Dharti H. Patel	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14 and 26* is/are allowed.

6)☒ Claim(s) *1-9,11 and 15-23* is/are rejected.

7)☒ Claim(s) *10,12,13,24 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/19/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Fujii et al., Patent No. 6,747,776.

With respect to claim 1, Fujii teach an integrated circuit [Fig. 6A, 60] comprising a first sub-circuit [Fig. 6A, 4] coupled to a first power supply rail [Fig. 6A, Vm1] providing a first power supply voltage; a second sub-circuit [Fig. 6A, 5] coupled to a second power supply rail [Fig. 6A, Vm2] providing a second power supply voltage; and a first power supply modulator [Fig. 6A, 1st Modulator 2], coupled to the first sub-circuit [Fig. 6A, 4], the modulator modulating the first power supply voltage without modulating the second power supply voltage [Col. 1, lines 20-24, Col. 9, lines 56 – Col. 10, lines 4].

With respect to claim 2, Fujii teaches that the first power supply modulator [Fig. 6A, 1st Modulator 2] comprises means for increasing the first power supply voltage [Col. 9, lines 56 – Col. 10, lines 4].

With respect to claim 3, Fujii teaches that the first power supply modulator [Fig. 6Am 1st Modulator 2] comprises means for decreasing the first power supply voltage [Col. 9, lines 56 – Col. 10, lines 4].

With respect to claim 4, Fujii teaches that the integrated circuit [Fig. 6A, 60] further comprises a second power supply modulator [Fig. 6A, 2nd Modulator 3], coupled to the second sub-circuit [Fig. 6A, 5], the second modulator modulating the second power supply voltage without modulating the first power supply voltage [Col. 1, lines 20-24, Col. 9, lines 56 – Col. 10, lines 4].

With respect to claim 15, Fujii teaches a0n integrated circuit [Fig. 6A, 60] including a first sub-circuit [Fig. 6A, 4] coupled to a first power supply rail [Fig. 6A, Vm1] providing a first power supply voltage and a second sub-circuit [Fig. 6A, 5] coupled to a second power supply rail [Fig. 6A, Vm2] providing a second power supply voltage, the method comprising the steps of (A) receiving a trigger signal [Fig. 6A, LTs]; and (B) in response to receipt of the trigger signal, modulating the first power supply voltage without modulating the second power supply voltage [Col. 1, lines 20-24, Col. 9, lines 56 – Col. 10, lines 4].

With respect to claim 16, Fujii teaches that the step of (B) comprises a step of increasing the first power supply voltage [Col. 9, lines 56 – Col. 10, lines 4].

With respect to claim 17, Fujii teaches that the step (B) comprises a step of decreasing the first power supply voltage [Col. 9, lines 56 – Col. 10, lines 4].

With respect to claim 18, Fujii further comprising a step of (C) in response to receipt of the trigger signal [Fig. 6A, LTs], modulating the second power supply voltage [Fig. 6A, Vm2] without modulating the first power supply voltage.

With respect to claim 19, Fujii teaches that the step (B) comprises a step of modulating [Fig. 6A, 1st Modulator] the first power supply voltage [Fig. 6A, Vm1] by a first amount, and wherein the step (C) comprises a step of modulating [Fig. 6A, 2nd Modulator] the second power supply voltage [Fig. 6A, Vm2] by a second amount which differs from the first amount.

With respect to claim 20, Fujii teaches that the step (B) comprises a step of modulating the first power supply voltage by a first amount, and wherein the step (C) comprises a step of modulating the second power supply voltage by a second amount which differs from the first amount [Col. 2, lines 45-48].

With respect to claim 21, Fujii teaches that steps (B) and (C) are performed contemporaneously [Two modulators, first and second modulators, are modulating the power supply voltage at the same time; Col. 2, lines 45-48].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii, in view of Miyazaki, Patent No. 5,083,096.

Fujii does not disclose an output identifier and a comparator. Miyazaki teaches an integrated circuit comprising an output identifier [Fig. 6, 24], coupled to the first sub-circuit [Fig. 6, 21], that identifies an actual output of the first sub-circuit [Fig. 6, 21] while the first power supply modulator [Fig. 6, 34] modulates the first power supply voltage [Fig. 6, 26]; and a comparator [Fig. 6, 25], coupled to the output identifier [Fig. 6, 24], that compares the actual output to an expected output of the first sub-circuit [Col. 3, lines 31-50].

Both teachings are analogous integrated circuits comprising power supply rails, modulators, and sub-circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Miyazaki, which teaches an output identifier and a comparator, with the integrated circuit of Fujii for the benefit of detecting the output level to produce a level detection signal representative of the output level.

With respect to claim 6, Miyazaki teaches that the first power supply modulator comprises at least one first shunt [Fig. 6, 21a] coupled to the first power supply rail [Fig. 6, 26].

With respect to claim 7, Miyazaki teaches that the at least one first shunt comprises at least one transistor [Fig. 6, 21a].

With respect to claim 8, Miyazaki further comprises a first shunt controller [Fig. 6, 23], coupled to the at least one first shunt [Fig. 6, 21a], that controls activation of the at least one first shunt.

With respect to claim 9, Miyazaki teaches that the first shunt controller [Fig. 6, 23] comprises means for activating the at least one first shunt [Fig. 6, transistor 21a] for a first predetermined period of time [Col. 3, lines 21-25].

With respect to claim 11, Miyazaki further comprises a trigger circuit [Fig. 6, IN] that provides a trigger signal to the first shunt control means [Fig. 6, 23]; and wherein the first shunt controller [Fig. 6, 23] comprises means for activating the at least one first shunt [Fig. 6, 21a] in response to receipt of the trigger signal [Col. 3, lines 21-25].

With respect to claim 22, Fujii does not disclose that the method further comprises steps of identifying an actual output of the first sub-circuit, and comparing the actual output to an expected output of the first sub-circuit.

Miyazaki teaches a method that comprises steps of identifying an actual output of the first sub-circuit [Fig. 6, Output level detection circuit 24] while the step (B) is being performed; and comparing [Fig. 6, Comparator 25] the actual output to an expected output of the first sub-circuit [Fig. 6, 21].

Both teachings are analogous integrated circuits comprising power supply rails, modulators, and sub-circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Miyazaki, which teaches an output identifier and a comparator, with the integrated circuit of Fujii for the benefit of detecting the output level to produce a level detection signal representative of the output level.

With respect to claim 23, Mayazaki teaches that the step (B) comprising a step of activating at least one first shunt [Fig. 6, 21a] for a first predetermined period of time, the at least one first shunt being coupled to the first power supply rail [Fig. 6, 26].

Allowable Subject Matter

3. Claims 10, 12-13,and 24-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for indicating allowance of claim 10 and 24: The prior art does not disclose that the first shunt comprises a first plurality of shunts, and wherein the first shunt controller comprises means for activating a predetermined subset of the first plurality of shunts.

The following is an examiner's statement of reasons for indicating allowance of claim 12: The prior art does not disclose that the second power supply modulator comprises at least one second shunt, a second shunt controller, the trigger circuit for providing the trigger signal to the second shunt control means; and that the second shunt controller comprises means for activating the at least one second shunt in response to receipt of the trigger signal. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.'

The following is an examiner's statement of reasons for indicating allowance of claim 13: The prior art does not disclose delay means for delaying the trigger signal by a predetermined delay and for providing the delayed trigger signal to the first shunt controller; and wherein the first shunt controller comprises means for activating the at least one first shunt in response to receipt of the delayed trigger signal. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

The following is an examiner's statement of reasons for indicating allowance of claim 25: The prior art does not disclose the step of prior to the step (B), delaying the trigger signal by a predetermined delay to produce a delayed trigger signal; wherein the step (A) comprises a step of receiving the delayed trigger signal; and wherein the step (B) comprises a step of modulating the first power supply voltage without modulating the second power supply voltage in response to receipt of the delayed trigger signal. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

4. Claims 14 and 26 are allowed.

The following is an examiner's statement of reasons for indicating allowance of claim 14: The prior art teaches a first sub-circuit, a second sub-circuit, but does not disclose a first plurality of shunts coupled to the first power supply rail and to the first sub-circuit to modulate the first power supply voltage without modulating the second power supply voltage; first shunt control means,

coupled to the first plurality of shunts, for activating a predetermined subset of the first plurality of shunts for a first predetermined period of time in response to receipt of a trigger signal; output identification means for identifying an actual output of the first-sub-circuit while the first power supply modulation means modulates the first power supply voltage; and comparison means, for comparing the actual output to an expected output of the first sub-circuit. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

The following is an examiner's statement of reasons for indicating allowance of claim 26: The prior art does not disclose the step of activating a subset of a first plurality of shunts for a first predetermined period of time to modulate the first power supply voltage by a first amount in response to receipt of the trigger signal; and in response to receipt of the trigger signal, activating a subset of a second plurality of shunts for a second predetermined period of time to modulate the second power supply voltage by a second amount which differs from the first amount; wherein the steps are performed contemporaneously. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DHP
11/20/2006

Stephen W Jackson
11-22-06

STEPHEN W. JACKSON
PRIMARY EXAMINER